

GSM823 离线语音识别

技术规格书 V1.0



GSM823 Features

CPU

- 32bit DSP
- Maximum speed 192MHz
- 8 Levels interrupt priority

Memory

- ROM
- Optional built-in flash memory

Clocks

- On-chip 16 MHz clock
- On-chip 200KHz lower-temperature-drift clock

DSP Audio Processing

- Multi-band EQ configuration for voice Effects

Audio Codec

- One channel 16-bit DAC
SNR $\geq$ 98dB@740mVrms
- One channel 16-bit ADC
SNR $\geq$ 95dB@1Vrms
- Audio DAC Sampling rates of
8KHz/11.025KHz/16KHz/22.05KHz/24KHz/ 32KHz/44.1KHz/48KHz/64KHz/88.2KHz/96KHz are supported
- Audio ADC Sampling rates of
8KHz/11.025KHz/16KHz/22.05KHz/24KHz/ 32KHz/44.1KHz/48KHz are supported
- Support AMUX and ADC to DAC

Peripherals

- One full speed USB OTG controller
- One SD host controller for MMC/SD
- Three multi-function 32-bit timers, support capture and PWM mode
- UART controller supports DMA
- One IIC Master controller
- One SPI Master / Slaver controller with DMA
- One QDEC interface
- 5-channel 10-bit general purpose ADC
- Two pairs MCPWM
- 5 Individually programmable and multiplexed GPIO pins
- Digital peripheral crossbar
- Up to 5 external interrupt / wake-up source (low power available, can be multiplexed to any I/O)

PMU

- VPWR range : 2.7V to 5.5V
- IOVDD range : 2.1V to 3.6V

Packages

- SOP8

Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

Applications

- Audio player
- Microcontrollers



1 Block Diagram

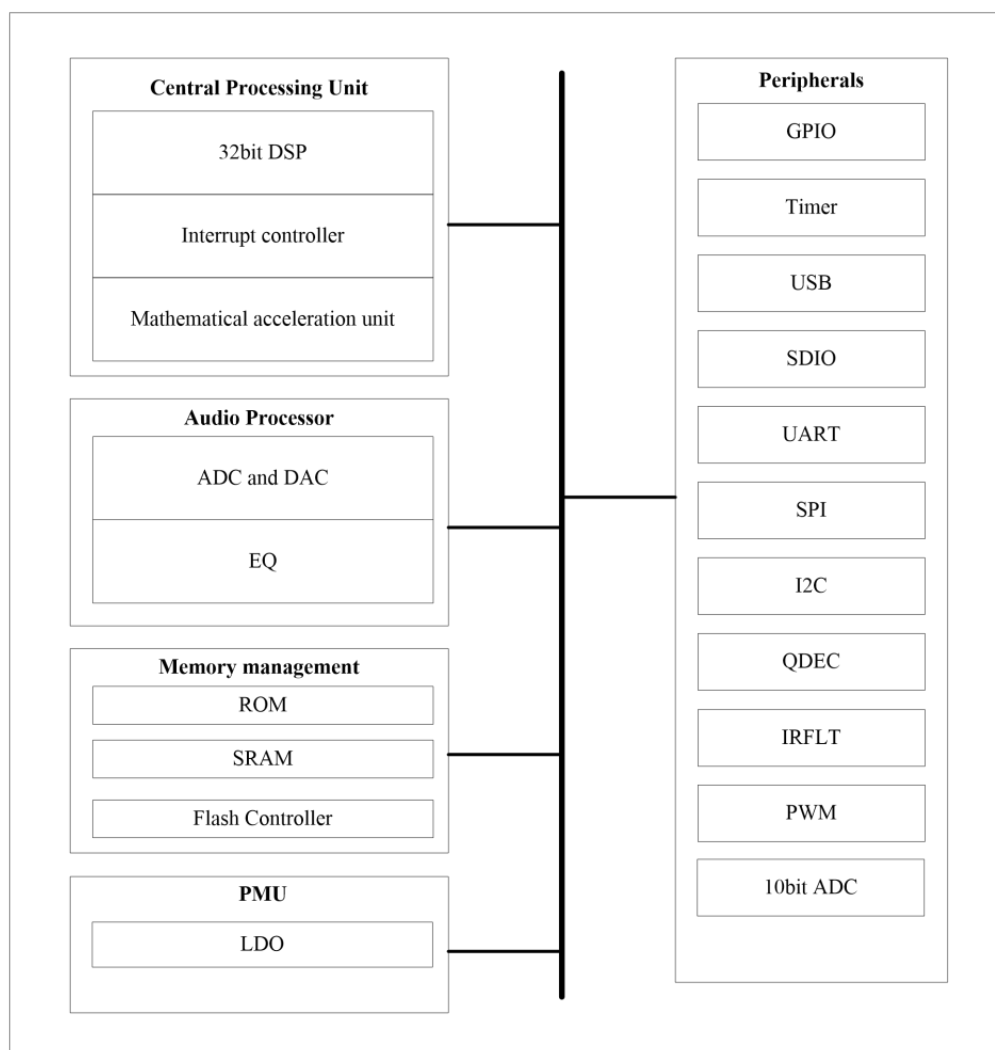


Figure 1-1 GSM823 Block Diagram



2 Pin Definition

2.1 Pin Assignment

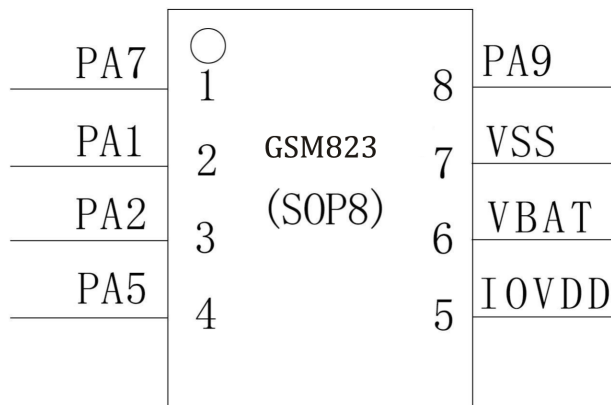


Figure 2-1 GSM823 Package Diagram



2.2 Pin Description

Table 2-1 GSM823 Pin Description

PIN NO.	Name	Type	Function	Other Function
1	DACL	AO		Left channel audio output;
	PA7	I/O	GPIO	ADC7:ADC Input Channel 7; MICIN:MIC Input Channe; AUX1:Analog input Channel 1;
2	PA1	I/O	GPIO (pull up)	Long press reset; MCLR; ADC1:ADC Input Channel 1;
	PA4	I/O	GPIO	ADC4:ADC Input Channel 4; SPIOCLK(B):SPIO Clk(B);
	PA14	I/O	GPIO (VPP)	
3	PA2	I/O	GPIO	ADC2:ADC Input Channel 2; SPIODI(B):SPIO Data In(B);
	PA3	I/O	GPIO	ADC3:ADC Input Channel 3; SPIOD0(B):SPIO Data Out(B);
	UDBDM	I/O	USB Negative Data (pull down)	ADC15:ADC Input Channel 15;
4	USBDP	I/O	USB Positive Data (pull down)	ADC14:ADC Input Channel 14;
	PA0	I/O	GPIO	ADC0:ADC Input Channel 0;
	PA5	I/O	GPIO	ADC5:ADC Input Channel 5; AUX3:Analog input Channel 3; SPIOCS(B):SPIO Chip Select(B);
5	IOVDD	PO	Power supply for GPIO	Built-in linear voltage regulator output;
6	VPWR	PI		Power supply input;
7	VSS	G		System ground;
8	PA8	I/O	GPIO	ADC8:ADC Input Channel 8; AUX0:Analog input Channel 0;
	PA9	I/O	GPIO	ADC9:ADC Input Channel 9; MICLDO:MIC linear voltage regulator output; MIC_BIAS:MIC Bias Output(Built-in resistor);

Pin Type	Description	Pin Type	Description
P	Power	I/O	Input or Output
PI	Power Input	AO	Analog Output
PO	Power Output	G	Ground



CROSSBAR						
SPI1	SDC	IIC	Q-decoder	UART0	UART1	MCPWM
SPI1_CLK	SD_CLK	IIC_CLK	Q-decoder 0	UART0_TX	UART1_TX	PWMCH0H
SPI1_DI	SD_CMD	IIC_DAT	Q-decoder 1	UART0_RX	UART1_RX	PWMCH0L
SPI1_D0	SD_DAT				UART1_CTS	PWMCH1H
SPI1_DAT2					UART1_RTS	PWMCH1L
SPI1_DAT3						M_TMR0CK
						M_TMR1CK

Input Channel x8			Output Channel x8	
Timer0	CAP0	IRFLT	PWM0	CLK_OUT0
Timer1	CAP1		PWM1	CLK_OUT1
Timer2	CAP2		PWM2	CLK_OUT2
				CLK_OUT3



3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1

Symbol	Parameter	Min	Max	Unit
T _{opt}	Operating temperature	-40	+85	° C
T _{stg}	Storage temperature	-65	+150	° C
VPWR	Power supply input	-0.3	6.0	V
V _{IOVDD}	Voltage applied at IOVDD	-0.3	3.6	V
V _{GPIO}	Voltage applied to GPIO	-0.3	IOVDD+0.3	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

3.2 ESD Protectio

Table 3-2

Parameter	Typ.	Test pin	Reference standard
Human Body Mode	±4KV	All pins	JEDEC EIA/JESD22-A114
Machine Mode	±200V	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±2KV	All pins	JEDEC EIA/JESD22-C101F
Latch up	±200mA	All GPIO pins	JEDEC STANDARD NO. 78E
	1.5xV _{opmax}	All power pins	

Note : 1.5xV_{opmax} = 1.5 times maximum operating voltage.

3.3 PMU Characteristics

Table 3-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VPWR	Charger supply Voltage	2.7	5.0	5.5	V	—
IOVDD	Voltage output	2.1	3.0	3.6	V	VPWR = 4.2V, 10mA loading
	Loading current	—	—	100	mA	IOVDD=3.3V@VPWR = 3.6V
V _{LVD}	Voltage input	1.8	2.5	2.5	V	Low-Voltage Detection of IOVDD



3.4 IO Input/Output Electrical Logical Characteristics Table

3-4

GPIO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Low-Level Input Voltage	-0.3	—	$0.3 \times IOVDD$	V	$IOVDD = 3.0V$
V_{IH}	High-Level Input Voltage	$0.7 \times IOVDD$	—	$IOVDD + 0.3$	V	$IOVDD = 3.0V$
GPIO output characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}	Low-Level Input Voltage	—	—	$0.1 \times IOVDD$	V	$IOVDD = 3.0V$
V_{OH}	High-Level Input Voltage	$0.9 \times IOVDD$	—	—	V	$IOVDD = 3.0V$

3.5 IO Output Drive Strength Pull Up/Down Characteristics

Table 3-5

Port	Drive Strength	Pull Up Resistance	Pull DownResistance	Test Conditions
PA0~PA5 PA7~PA9	00: 2mA 01: 6mA 10: 18mA 11: 45mA	10K/100K/1M	10K/100K/1M	$IOVDD = 3.3V$
PA14	8mA	10K/100K/1M	10K/100K/1M	$IOVDD = 3.3V$
DP	8mA	1.5K	15K	$IOVDD = 3.3V$
DM	8mA	180K	15K	$IOVDD = 3.3V$

Note1: precision of 10K/100K pull-up and pull-down resistor is $\pm$

30% Note2: precision of 1M pull-up and pull-down resistor is $\pm 50\%$

Note3: PA1 default pull up, USBDM and USBDP default pull down



3.6 Audio DAC Characteristics

Table 3-6

Parameter	Min	Typ	Max	Unit	Test Conditions
Frequency Response	20	—	20K	Hz	VPWR=5.0V Fin=1KHz/0dB Fin=1KHz/-60dB B/W=20Hz~20kHz A-Weighted Filter 10k ohm loading
Output Swing	—	740	—	mVrms	
THD+N	—	-77	—	dB	
S/N	—	98	—	dB	
Dynamic Range	—	92	—	dB	
Noise Floor	—	10	—	uVrms	

3.7 Audio ADC Characteristics

Table 3-7

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range	—	72	—	dB	Gain=23dB Fsample=44.1KHz Fin=1KHz @57mVrms A-Weighted Filter B/W=20Hz-20KHz
S/N	—	71	—	dB	
THD+N	—	-68	—	dB	



4 Package Information

4.1 SOP8

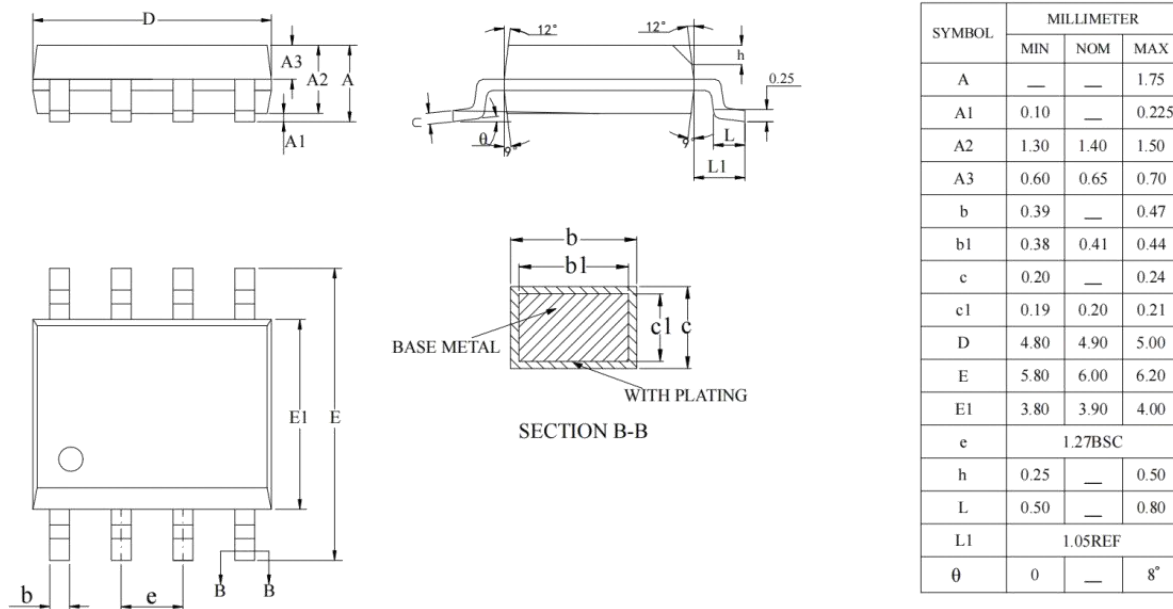


Figure 4-1 GSM823 Package



5 Solder-Reflow Condition

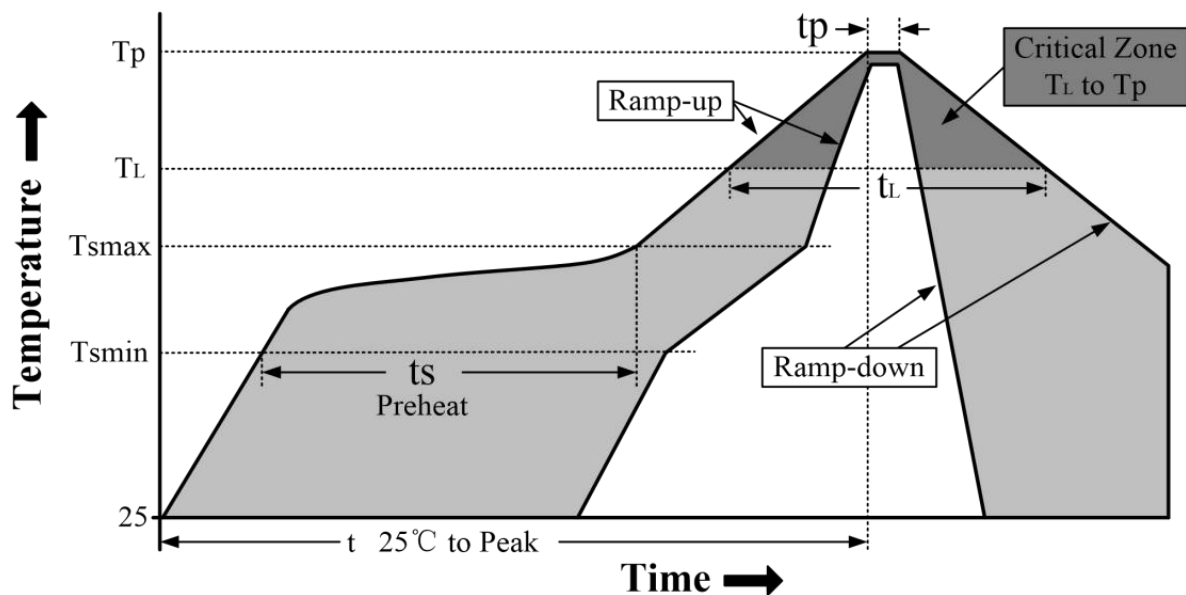


Figure 5-1 Classification Reflow Profile

Classification Profiles

Table 5-1

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat / Soak	Temperature Min (T_{min})	100 °C	150 °C
	Temperature Max (T_{max})	150 °C	200 °C
	Time (t_s) from (T_{min} to T_{max})	60-120 seconds	60-180 seconds
Average ramp-up rate (T_{max} to T_p)		3 °C/second max	3 °C/second max
Liquidous temperature (T_L)		183 °C	217 °C
Time (t_L) maintained above T_L		60-150 seconds	60-150 seconds
Peak package body temperature (T_p)		See Table 5-2.	See Table 5-3.
Time within 5° C of actual Peak Temperature (t_p)		10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)		6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature		6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5°C of actual peak temperature (t_p) specified for the reflow profiles is a “supplier” minimum and “user” maximum.

SnPb - Classification Temperature

Table 5-2

Package Thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
< 2.5 mm	240 +0/-5 °C	225 +0/-5 °C
≥ 2.5 mm	225 +0/-5 °C	225 +0/-5 °C



Pb-free - Classification Temperature

Table 5-3

Package Thickness	Volume mm ³ < 350	Volume mm ³ 350 - 2000	Volume mm ³ > 2000
< 1.6mm	260 °C	260 °C	260 °C
1.6 mm - 2.5mm	260 °C	250 °C	245 °C
> 2.5mm	250 °C	245 °C	245 °C



6 Storage Condition

6.1 Moisture Sensitivity Level

GSM823 is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-033.

6.2 Storage Alert

1. Calculated shelf life in sealed bag 12 months at $<40^{\circ}\text{C}$ and 90% relative humidity (RH).
 2. Peak package body temperature $\leq 260^{\circ}\text{C}$.
 3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be mounted within 168 hours of factory conditions $\leq 30^{\circ}\text{C}/60\%\text{RH}$ or stored per J-STD-033.
 4. Devices require bake before mounting if humidity indicator card reads $> 10\%$ for level 2a-5a devices or $> 60\%$ for level 2 devices when read at $23 \pm 5^{\circ}\text{C}$, or 3a or 3b are not met.
- Please refer to IPC/JEDEC J-STD-033 for baking procedure if necessary.



7 Revision History

Date	Revision	Description
2024.01.05	V1.0	Initial Release.

